Please add new Claims 22 and 23.

22. (New) A crosspoint switch as claimed in claim 1 wherein the input buses and the output buses are differential data lines, and further comprising data-line-to-data-line precharge circuits that share charge between the data lines to a midpoint of voltage swing on the data lines.

#4

23. (New) A method as claimed in claim 13 wherein the input buses and the output buses are differential data lines, and further comprising precharging the differential buses through a data-line-to-data-line precharge circuit that shares charge between the data lines to a midpoint of voltage swing on the data lines.

## REMARKS

An Information Disclosure Statement (IDS) is being filed concurrently herewith. Entry of the IDS is respectfully requested.

Claims 5 and 11 were rejected under 35 U.S.C. 112, second paragraph due to the use of the term "similar." Each of those claims has been amended to overcome that rejection. Support for the term "tracks" can be found in the specification at page 10, line 20 through page 11, line 2.

All claims were rejected under 35 U.S.C. 103 as being unpatentable over Upp, U.S. 4,914,429 in view of Bridgewater, U.S. 6,034,551 alone or in combination with Dupcak et al., U.S. 6,414,520 or Lukes et al., U.S. 6,218,901. Those rejections are respectfully traversed and reconsideration is requested.

The prior art citations which relate to crosspoint switches are the Upp Patent 4,914,429, on which the Examiner relies, and the Shin and Hodges article cited by Applicant. As shown in Fig. 2 of Upp, each crosspoint of that switch comprises an AND gate 65a-a to 65p-p. An

additional OR gate 67a to 67p connects the outputs of the AND gates in each column. The crosspoint switch of Upp has the advantage of a very simple gate circuit at each crosspoint.

Shin and Hodges improved upon the crosspoint gate approach in order to reduce power. As illustrated in Fig. 7, each crosspoint comprises four transistors MPS1, MPS2, MNS2 and MNS1. Transistors MPS1 and MNS1 form an inverter, the output of which is passed by transistors MPS2 and MNS2. To improve power consumption, the output of each column includes a voltage swing limiter (Fig. 5) which takes the form of the static trans-resistance amplifier show in Fig. 6 and to the right of Fig. 7. Again, Shin and Hodges have the advantage of a very simple circuit at each crosspoint.

Compare the simple crosspoint of four transistors in Shin and Hodges with the more complex crosspoint circuit of the embodiment of Fig. 20 of the present application. In this embodiment, all of the transistors within the regenerative amplifier 119 and the driver circuit 223 of the modified repeater 217 replace the four transistor circuit of Shin and Hodges. By using a clocked regenerative amplifier in the crosspoint, a very low swing signal on the input bus can be sensed at the crosspoint, and the low swing driver 223 repeats the sensed signal on the output lines. This more complex circuit enables low swing drive of both the input buses and the output buses for a substantial reduction in power requirements. It is counter-intuitive that the more complex, active amplifier and driver circuit would result in a reduction in power requirements when replacing the simple circuit of Shin and Hodges, or even the AND gates of Upp.

There is no suggestion in any prior art reference of the substantial power consumption gains which can be obtained using more complex crosspoint circuitry which enables low swing signals in both the input and output buses. In particular, there is no suggestion of placing an amplifier, particularly a clocked regenerative amplifier, and a low swing driver circuit in the crosspoint. Nor is there any suggestion, in a crosspoint switch, of the more detailed claims of the present application.

For various teachings of differential and low swing signaling and amplifiers, the Examiner has cited the Bridgewater, Dupcak and Lukes patents. Applicant recognizes that the basic building blocks of H-bridge drivers, clocked amplifiers and differential signaling are well know. However, there is no suggestion in the prior art of using such circuits at crosspoints of a crosspoint switch or of the particular ways in which such circuits have been arranged in the present invention. One can only suggest such use in a crosspoint in hindsight based on the teachings of the present invention. In fact, the cited crosspoint switch references teach away from such complex circuitry, and the AND gates used in the crosspoints of Upp and the inverters used in the crosspoints of Shin and Hodges are not compatible with the low voltage differential signaling of any of the cited references.

Relative to claim 4, the Examiner has pointed to Figure 3 of Upp as showing a clock regenerative amplifier. The overall circuit of Figure 3 is a clock regenerator, and it includes an amplifier 87. However, the circuit is not clocked, and there is no regenerative amplifier. In Figure 3, the clock signal CK is itself being shaped and does not serve as a clock to an amplifier. Further, the circuit of Figure 3 is not within a crosspoint of the switch. The circuit of Figure 3 is in a circuit 40 of Figure 1 (column 4, lines 59-61) and is used to sense the duty factor of an output clock to enable duty factor correction. The circuit is not found at the crosspoints which are within the switching matrices 60. No clock signal is applied to the crosspoints in either Upp or Shin and Hodges. There is no suggestion of a clocked regenerative amplifier at a crosspoint.

## CONCLUSION

In view of the above amendments and remarks, it is believed that all claims are in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned at (978) 341-0036.

Respectfully submitted,

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Dated: 7/26/3

MARKED UP VERSION OF AMENDMENTS

Specification Amendments Under 37 C.F.R. § 1.121(b)(1)(iii)

Replace the paragraph at page 2, lines 9 through 15 with the below paragraph marked up by way of bracketing and underlining to show the changes relative to the previous version of the paragraph.

In accordance with the present invention, a crosspoint switch comprises a plurality of input buses on which signals are driven at low swing and a plurality of output buses on which signals are driven at low swing. Each of a plurality of crosspoints selectively passes a signal from a low swing input bus to a low swing output bus.

[Specifically,] In specific embodiments, at the crosspoints, low swing signals on the input buses are sensed, and the signals are driven on the output buses at low swing. Low swing signals on the output buses are then sensed at an output.



Claim Amendments Under 37 C.F.R. § 1.121(c)(1)(ii)

5. (Amended) A crosspoint switch as claimed in claim 4 further comprising a timing circuit which controls timing of the crosspoint switch from a clock, the timing circuit including a delay, the timing of which tracks [varies in a manner similar to] timing variations in the driver circuit.

11. (Amended) A crosspoint switch as claimed in claim 10 further comprising a timing circuit which controls timing of the crosspoint switch from a clock, the timing circuit including a delay, the timing of which tracks [varies in a manner similar to] timing variations in the driver circuit.